Curriculum Vitae

PERSONAL INFORMATION

Marco Lanuzza

Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica (DIMES)
Università della Calabria
Via P. Bucci, 42C I-87036, Rende (CS), Italy.

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Sex Male | Nationality Italian

EDUCATION

APRIL 2005 — Ph.D. degree in Electronic Engineering
Università degli Studi "Mediterranea" di Reggio Calabria, Reggio Calabria, Italy.

NOVEMBER 2000 — M.S. degree in Electronic Engineering with full grade (110/110)
Università degli Studi "Mediterranea" di Reggio Calabria, Reggio Calabria, Italy.

JULY 1993 — "Diploma di maturità scientifica" with full grade (60/60)
Liceo Scientifico L. da Vinci, Reggio Calabria, Italy.

EMPLOYMENT HISTORY

APRIL 2019 - PRESENT — Associate Professor of Electronics
Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica (DIMES), University of Calabria, Rende (CS), Italy.

MAY 2006 – MARCH 2019 — Assistant Professor of Electronics
Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica (DIMES), University of Calabria, Rende (CS), Italy.

APRIL 2005 - APRIL 2006 — Postdoc Researcher
Dipartimento di Elettronica Informatica e Sistemistica (DEIS), University of Calabria, Rende (CS), Italy.

NOVEMBER 2004 - MARCH 2005 — Research Contract
Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica (DIMES), University of Calabria, Rende (CS), Italy.

JUNE 2004 - SEPTEMBER 2004 — Visiting Researcher
Department of Electrical and Computer Engineering, University of Rochester, Rochester (NY), USA.

MARCH 2001 - JUNE 2002 — Staff Hw Engineer
R&D Tetra-Radiomobile division, Marconi Mobile S.P.A, Sestri Ponente (GE), Italy.

RESEARCH ACTIVITY

RESEARCH INTERESTS

My general research interests focus on high-performance and low-power digital and mixed-signal VLSI circuits, particularly addressing nano-meter design issues pertaining to power, performance and robustness. My aim is to develop novel circuit techniques for effective circuit design, in conjunction with efficient and accurate analysis and optimization methods.
My current research activity concerns the following main topics:

- **High Performance Digital and Mixed-Signal VLSI/ICs**
- **Design of ultra-low power CMOS Digital and Mixed-Signal circuits and systems**
- **Design of digital and analog/mixed-signal circuits in emerging technologies**

RESEARCH ID

Researcher ID: K-1294-2013
Scopus Author ID: 9738181600
ORCID ID: orcid.org/0000-0002-6480-9218

PARTICIPATION IN RESEARCH PROJECTS

"Diodi spintronici rad-hard ad elevata sensitività (DIOSPIN)"
Tipologia: Progetto finanziato dall' Agenzia Spaziale Italiana (ASI), bando 2017 "NUOVE IDEE PER LA COMPONENTISTICA SPAZIALE DEL FUTURO"
Duration:24 months
Role: Principal Investigator

"Progettazione e sviluppo di sensori spintronici per imaging a microonde con applicazione ai test non distruttivi e alla caratterizzazione dei materiali"
Tipologia: progetto di ricerca finanziato dalla Fondazione Cassa di Risparmio di Calabria e Lucania - Progetto n.17/Ricerca Scientifica e Tecnologica
Duration:24 months
Role: Principal Investigator

MI 01_00052 "WEBS - SISTEMA INTEGRATO WIRELESS MULTIFUNZIONALE PER LA GESTIONE DELL'ENERGIA, DEL BENESSERE E DELLA SICUREZZA" Capofila: Beghelli S.p.A. - Bando Industria 2015 "Made in Italy". finanziato da MISE
Duration:36 months
Role: Researcher

PON01_01503 "Sistemi integrati per il monitoraggio, l'early-warning e la mitigazione del rischio idrogeologico lungo le grandi vie di comunicazione" Capofila: UNICAL - Autostrade Tech. S.p.A. - finanziato da MIUR
Duration:36 months
Role: Researcher

EE01_0006 "SISTEMI FOTOVOLTAICI, AD ALTA CONCENTRAZIONE ED ELEVATA EFFICIENZA, FORTEMENTE INNOVATIVI ED INTEGRATI, DOTATI DI INSEGUITORI SOLARI, DIAGNOSTICA EVOLUTA E GESTIONE DELL'ENERGIA PER L'IMMISSIONE DELL'ELETTRICITA' NELLA RETE PUBBLICA" Capofila: Beghelli S.p.A. - Bando Industria 2015 "Efficienza Energetica". finanziato da MISE - Azione "Efficienza Energetica"
Duration:36 months
Role: Researcher

"MODERN: MOdeling and DEsign of Reliable, process variation-aware Nanoelectronic devices, circuits and systems" Programma Cooperativo Europeo JTI ENIAC 120003 - MIUR 4825/E.
Duration:36 months
Role: Researcher

Progetto di ricerca nazionale dal titolo: "Compressore wavelet real time per immagini ad alta risoluzione". Codice del progetto: n. 7543. Bando Fondo per le Agevolazioni alla Ricerca del Ministero dell'Istruzione, dell'Università e della Ricerca
Duration:36 months
Role: Researcher

Progetto n. 2.1.4 "Ricerca su celle fotovoltaiche innovative", finanziato da ENEA nell'ambito dell'Accordo di Programma Ministero dello Sviluppo Economico -ENEA: Attività di Ricerca e Sviluppo di Interesse Generale per il Sistema Elettrico Nazionale
Duration:12 months
Role: Researcher

PUBBLICATIONS

INTERNATIONAL JOURNALS

1. Garzon E., De Rose R., Crupi F., Carpentieri M., Teman A., **Lanuzza M.**. (in press),"Simulation Analysis of DMTJ-Based STT-MRAM Operating at Cryogenic Temperatures", IEEE

TRANSACTIONS ON MAGNETICS, ISSN: 0018-9464, doi: 10.1109/TMAG.2021.3073861

2. Fassio L., Settino F., Lin L., De Rose R., **Lanuzza M.**., Crupi F., Alioto M. (2021),"A Robust, High-Speed and Energy-Efficient Ultralow-Voltage Level Shifter", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, ISSN: 1549-7747, vol. 68, issue 4, April 2021, doi: 10.1109/TCSII.2020.3033253
3. Garzon E., De Rose R. , Crupi F., Teman A., **Lanuzza M.**. (2021),"Exploiting STT-MRAMs for Cryogenic Non-Volatile Cache Applications", IEEE TRANSACTIONS ON NANOTECHNOLOGY, ISSN: 1941-0085, vol. 20, January 2021, pp. 123 – 128, doi: 10.1109/TNANO.2021.3049694
4. Puliafito V., De Rose R. , Crupi F., Chiappini S., Finocchio G., **Lanuzza M.**., Carpentieri M. (2020),"Impact of Scaling on Physical Unclonable Function based on Spin-Orbit Torque", IEEE Magnetics Letters, ISSN: 1949-3088, vol. 11, ASN: 4505205, September 2020, doi: 10.1109/LMAG.2020.3025263
5. Shavit N., Stanger I., Taco R., **Lanuzza M.**., Fish A. (2020), "A 0.8V, 1.54 pJ / 940 MHz Dual Mode Logic-based 16×16-bit Booth Multiplier in 16-nm FinFET", IEEE Solid-State Circuits Letters, ISSN: 2573-9603, vol.3, July 2020, pp. 314 – 317, doi: 10.1109/LSSC.2020.3011636
6. Stanger I., Shavit N., Taco R., **Lanuzza M.**., Fish A. (2020),"Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, ISSN: 1549-7747, vol. 67, issue 9, Sept. 2020, pp. 1639 – 1643, doi: 10.1109/TCSII.2020.3013331
7. Finocchio G., Moriyama T., De Rose R., Siracusano G., **Lanuzza M.**., Puliafito V., Chiappini S., Crupi F., Zeng Z., Ono T., Carpentieri M. (2020),"Spin–orbit torque based physical unclonable function", AIP Journal of Applied Physics, ISSN: 0021-8979, vol. 128, issue 3, July 2020, Article number 13408, doi: 10.1063/5.0013408
8. Garzon E., De Rose R., Crupi F., Trojman L., Finocchio G., Carpentieri M., **Lanuzza M.**. (2020), "Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework", INTEGRATION, the VLSI journal, ISSN: 0167-9260, vol. 71, March 2020, pp. 56–69, doi: 10.1016/j.vlsi.2020.01.002
9. De Rose R, D'Aquino M, Finocchio G, Crupi F, Carpentieri M, **Lanuzza M.** (2019). Compact Modeling of Perpendicular STT-MTJs with Double Reference Layers. IEEE TRANSACTIONS ON NANOTECHNOLOGY, ISSN: 1941-0085, vol. 18, issue 1, December 2019, pp. 1063 – 1070, doi: 10.1109/TNANO.2019.2945408
10. Garzon E, De Rose R., Crupi F, Trojman L, **Lanuzza M.** (2019). Assessment of STT-MRAM performance at nanoscaled technology nodes using a device-to-memory simulation framework. MICROELECTRONIC ENGINEERING, ISSN: 0167-9317, vol. 215, article number 111009, July 2019, doi: 10.1016/j.mee.2019.111009
11. Taco R, Levi I, **Lanuzza M.**, Fish A (2019). An 88-fJ/40-MHz [0.4V] – 0.61-pJ/1-GHz [0.9V] Dual-Mode Logic 8×8 bit Multiplier Accumulator With a Self-Adjustment Mechanism in 28-nm FD-SOI. IEEE JOURNAL OF SOLID STATE CIRCUITS, ISSN: 0018-9200, vol. 54, issue 2, February 2019, pp. 560 – 568, doi: 10.1109/JSSC.2018.2882139
12. De Rose R , Romero P, **Lanuzza M.** (2019). Double-precision Dual Mode Logic Carry-Save Multiplier. INTEGRATION, the VLSI journal, ISSN: 0167-9260, vol. 64, January 2019, pp. 71–77, doi: 10.1016/j.vlsi.2018.08.003
13. Strangio S, Settino F, Palestri P, **Lanuzza M.**, Crupi F, Esseni D, Selmi L (2018). Digital and analog TFET circuits: design and benchmark. SOLID-STATE ELECTRONICS, ISSN: 0038-1101, vol. 146, August 2018, pp. 50–65, doi: 10.1016/j.sse.2018.05.003, (INVITED Review)
14. Crupi F, De Rose R, Paliy M, **Lanuzza M.**, Perna M, Iannaccone G (2018). A Portable Class of 3-Transistor Current References with Low-Power Sub-0.5 V Operation. INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, ISSN: 0098-9886, vol. 46, issue 4, April 2018, pp. 779-795, doi: 10.1002/cta.2439
15. De Rose R, **Lanuzza M.**, Crupi F, Siracusano G, Tomasello R, Finocchio G, Carpentieri M, Alioto M (2018). Variation-Aware Timing-Modeling Approach for Write Operation in Hybrid CMOS/STT-MTJ Circuits. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, ISSN: 1549-8328, vol. 65, iusse 3, March 2018, doi: 10.1109/TCSI.2017.2762431 (INVITED)
16. **Lanuzza M.**, Crupi F, Rao S, De Rose R, Iannaccone G (2017). Low Energy/Delay Overhead Level Shifter for Wide-Range Voltage Conversion. INTERNATIONAL JOURNAL OF CIRCUIT

THEORY AND APPLICATIONS, ISSN: 0098-9886, vol. 45, Issue 11, November 2017 , pp. 1637-1646, doi: 10.1002/cta.2294

17. Guerra N, De Rose R, Guevara M, Procel P, **Lanuzza M.**, Crupi F (2017). Understanding the impact of point-contact scheme and selective emitter in a c-Si BC-BJ solar cell by full 3D numerical simulations. SOLAR ENERGY, ISSN: 0038-092X, vol. 155, October 2017, pp. 1443–1450, doi: 10.1016/j.solener.2017.07.051
18. De Rose R, **Lanuzza M.**, d'Aquino M, Carangelo G, Finocchio G, Crupi F, Carpentieri M (2017). Compact Model with Spin-Polarization Asymmetry for Nanoscaled Perpendicular MTJs. IEEE TRANSACTIONS ON ELECTRON DEVICES, ISSN: 0018-9383, vol. 64, issue 10, October 2017, pp. 4346 – 4353, doi: 10.1109/TED.2017.2734967
19. **Lanuzza M.**., Crupi F., Rao S., De Rose R., Iannaccone G. (in press); *"Low energy/delay overhead level shifter for wide-range voltage conversion"*. JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, ISSN: 0098-9886, doi: 10.1002/cta.2294
20. Settino F., **Lanuzza M.**., Strangio S., Crupi F., Palestri P., Esseni D., Selmi L. (2017), *"Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits"*. IEEE TRANSACTIONS ON ELECTRON DEVICES, ISSN: 0018-9383, vol. 64, issue 6, June 2017, pp. 2736 – 2743, doi: 10.1109/TED.2017.2689746
21. Procel P., Ingenito A., De Rose R., Pierro S., Crupi F., **Lanuzza M.**., Cocorullo G., Isabella O., Zeman M. (2017); *"Opto-electrical modelling and optimization study of a novel IBC c-Si Solar Cell"*. PROGRESS IN PHOTOVOLTAICS: RESEARCH AND APPLICATIONS, ISSN: 1099-159X, vol. 25, issue 6, June 2017, pp. 452–469, doi: 10.1002/pip.2874
22. De Rose R., **Lanuzza M.**., Crupi F., Siracusano G., Tomasello R., Finocchio G., Carpentieri M. (2017); *"Variability-Aware Analysis of Hybrid MTJ/CMOS Circuits by a Micromagnetic-Based Simulation Framework"*. IEEE TRANSACTIONS ON NANOTECHNOLOGY, ISSN: 1941-0085, vol. 16, issue 2, March 2017, pp. 160-168, doi: 10.1109/TNANO.2016.2641681
23. De Rose R., Crupi F., **Lanuzza M.**., Albano D. (2017); *"A physical unclonable function based on a 2-transistor subthreshold voltage divider"*. JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, vol. 45, issue 2, February 2017, pp. 260-273, ISSN: 0098-9886, doi: 10.1002/cta.2282
24. Strangio S., Palestri P., **Lanuzza M.**., Esseni D., Crupi F., Selmi L. (2017); *"Benchmarks of a III-V TFET technology platform against the 10-nm CMOS FinFET technology node considering basic arithmetic circuits"*. SOLID-STATE ELECTRONICS, ISSN: 0038-1101, vol. 128, February 2017, pp. 37–42, doi: 10.1016/j.sse.2016.10.022
25. **Lanuzza M.**., Crupi F., Rao S., De Rose R., Strangio S., Iannaccone G. (2017); *"An Ultra-Low Voltage Energy Efficient Level Shifter"*. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, ISSN: 1549-7747, vol. 64, issue 1, January 2017, pp. 61-65, doi: 10.1109/TCSII.2016.2538724
26. Guevara M., Procel P., De Rose R., Guerra N., Crupi F., **Lanuzza M.**. (2016); *"Design guidelines for a metallization scheme with multiple-emitter contact lines in BC-BJ solar cells"*. JOURNAL OF COMPUTATIONAL ELECTRONICS, ISSN: 15698025, vol 15, issue 4, pp 1498–1504, December 2016, doi: 10.1007/s10825-016-0898-y
27. Strangio S., Palestri P., **Lanuzza M.**., Crupi F., Esseni D., Selmi L. (2016); *"Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits*". IEEE TRANSACTIONS ON ELECTRON DEVICES, ISSN: 0018-9383, vol. 63, issue 7, pp. 2749-2756, doi: 10.1109/TED.2016.2566614
28. Taco R., Levi I., **Lanuzza M.**., Fish A. (2016); *"Low Voltage Logic Circuits Exploiting Gate Level Dynamic Body Biasing in 28 nm UTBB FD-SOI"*. SOLID-STATE ELECTRONICS, Special Issue on PLANAR FULLY-DEPLETED SOI TECHNOLOGY, ISSN: 0038-1101, vol. 117, March 2016, pp. 185–192, doi: 10.1016/j.sse.2015.11.013
29. **Lanuzza M.**., Strangio S., Crupi F., Palestri P., Esseni D. (2015); *"Mixed Tunnel-FET/MOSFET Level Shifters: A New Proposal to Extend the Tunnel-FET Application Domain"*. IEEE TRANSACTIONS ON ELECTRON DEVICES, ISSN: 0018-9383, vol. 62, issue 12, pp. 3973–3979, doi: 10.1109/TED.2015.2494845
30. Albano D., **Lanuzza M.**., Taco R., Crupi F. (2015); *"Gate-level body biasing for subthreshold logic circuits: analytical modeling and design guidelines"*. INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, ISSN: 0098-9886, vol. 43, issue 11, pp. 1523–

1540, doi: 10.1002/cta.2016

31. Finocchio G., Ricci M., Tomasello R., Giordano A., **Lanuzza M.**., Puliafito V., Burrascano P., Azzerboni B., Carpentieri M. (2015); *"Skyrmion based microwave detectors and harvesting"*. APPLIED PHYSICS LETTERS, ISSN: 00036951, vol. 107, issue 26, Article number 262401, doi: 10.1063/1.4938539
32. Taco R., **Lanuzza M.**., Albano D. (2015); *"Ultra-low-Voltage Self-body-biasing Scheme and its Application to basic Arithmetic Circuits"*. VLSI DESIGN, ISSN: 1065-514X, vol. 2015, Article ID 540482, pp. 1-10, doi: 10.1155/2015/540482
33. **Lanuzza M.**., Corsonello P., Perri S. (2015); *"Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs"*. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, ISSN: 1063-8210, vol. 23, issue 2, pp. 388-391, doi: 10.1109/TVLSI.2014.2308400
34. Corsonello P., Frustaci F., **Lanuzza M.**., Perri S. (2014); *"Over/undershooting effects in accurate buffer delay model for sub-threshold domain"*. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, vol. 61, issue 5, pp. 1456-1464, ISSN: 1549-8328, doi: 10.1109/TCSI.2013.2285691
35. Perri S., **Lanuzza M.**., Corsonello P. (2014); *"Design of High-Speed Low-Power Parallel-prefix adder trees in nanometer technologies"*. INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, vol. 42, issue 7, pp. 731–743, ISSN: 0098-9886, doi: 10.1002/cta.1886
36. Frustaci F., **Lanuzza M.**., Perri S., Corsonello P. (2014); *"Analyzing noise robustness of wide fan-in dynamic logic gates under process variations"*. INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, ISSN: 0098-9886, vol. 42, issue 5, pp. 452–467, ISSN: 0098-9886, doi: 10.1002/cta.1862
37. De Rose R., **Lanuzza M.**., Frustaci F. (2014); *"Designing Dynamic Carry Skip Adders: Analysis and Comparison"*. CIRCUITS, SYSTEMS AND SIGNAL PROCESSING, vol. 33, issue 4, pp. 1019-1034, ISSN: 1531-5878, doi: 10.1007/s00034-013-9688-y
38. Corsonello P., **Lanuzza M.**., Perri S. (2014); *"Gate-level body biasing technique for high speed sub-threshold CMOS logic gates"*. INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, vol. 42, issue 1, pp. 65-70, ISSN: 0098-9886, doi: 10.1002/cta.1838
39. **Lanuzza M.**. (2013); *"A Simple Circuit Approach to Improve Speed and Power Consumption in Pulse-Triggered Flip-Flops"*. JOURNAL OF LOW POWER ELECTRONICS, vol. 9, issue 4, pp. 445-451, December 2013, pp. 445-451(7) ISSN: 1546-1998, doi:10.1166/jolpe.2013.1276
40. Magnone P, Tonini D., De Rose R., Frei M., Crupi F., **Lanuzza M.**., Sangiorgi E., Fiegna C. (2013); *"A Comparative Study of MWT Architectures by Means of Numerical Simulations"*. ENERGY PROCEDIA, vol. 38, pp. 131-136, ISSN:1876-6102, doi: 10.1016/j.egypro.2013.07.259
41. **Lanuzza M.**., Corsonello P., Perri S. (2012); *"Low-Power Level Shifter for Multi-Supply Voltage Designs"*. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, vol. 59, issue 12, pp.922-926, ISSN: 1549-7747, doi: 10.1109/TCSII.2012.2231037
42. **Lanuzza M.**., De Rose R., Frustaci F., Perri S., Corsonello P. (2012); *"Comparative analysis of yield optimized pulsed flip-flops"*. MICROELECTRONICS RELIABILITY, vol. 52, pp.1679-1689, ISSN: 0026-2714, doi: 10.1016/j.microrel.2012.03.024
43. Frustaci F., Perri S., **Lanuzza M.**., Corsonello P. (2012); *"Energy-efficient single-clock-cycle binary comparator"*. INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS, vol. 40, pp. 237-246, ISSN: 0098-9886, doi: 10.1002/cta.720
44. De Rose R., Van Wichelen K., Tous L., Das J., Dross F., Fiegna C., **Lanuzza M.**., Sangiorgi E., Uruena De Castro A., Zanuccoli M. (2012); *"Optimization of Rear Point Contact Geometry by Means of 3-D Numerical Simulation"*. ENERGY PROCEDIA, vol. 27, pp. 197-202, ISSN:1876-6102, doi: 10.1016/j.egypro.2012.07.051
45. **Lanuzza M.**., Frustaci F., Perri S., Corsonello P. (2011); *"Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations"*. JOURNAL OF LOW POWER ELECTRONICS AND APPLICATIONS, Special Issue on Selected Topics in Low Power Design - From Circuits to Applications, vol. 1, pp. 97-108, ISSN 2079-9268, doi:

10.3390/jlpea1010097

46. Purhoit S., **Lanuzza M.**., Margala M. (2010); *"Design Space Exploration of Split-Path Data Driven Dynamic Full Adder"*. JOURNAL OF LOW POWER ELECTRONICS, vol. 6, issue 4, pp. 469-481, ISSN: 1546-1998, doi: 10.1166/jolpe.2010.1096
47. **Lanuzza M.**., Zicari P., Frustaci F., Perri S., Corsonello P. (2010); *"Exploiting Self Reconfiguration Capability to Improve SRAM-based FPGA Robustness in Space and Avionics Applications"*. ACM TRANSACTIONS ON RECONFIGURABLE TECHNOLOGY AND SYSTEMS, vol. 4, issue 1, article No 8, ISSN: 1936-7406, doi: 10.1145/1857927.1857935
48. Purhoit S., La **Lanuzza M.**., Perri S., Corsonello P., Margala M. (2009); *"Design and evaluation of an energy-delay-area efficient datapath for coarse-grain reconfigurable computing systems"*. JOURNAL OF LOW POWER ELECTRONICS, vol. 5, issue 3, pp. 326-338, ISSN: 1546-1998, doi: 10.1166/jolpe.2009.1033
49. Frustaci F., **Lanuzza M.**., Zicari P., Perri S., Corsonello P. (2009); *"Designing High-Speed Adders in Power-Constrained Environments"*. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, vol. 56, pp. 172-176, ISSN: 1549-7747, doi: 10.1109/TCSII.2008.2010187
50. Frustaci F., **Lanuzza M.**., Zicari P., Perri S., Corsonello P. (2009); *"Low-power split-path data driven dynamic logic"*. IET CIRCUITS, DEVICES & SYSTEMS, vol. 3, pp. 303-312, ISSN: 1751-858X, doi: 10.1049/iet-cds.2009.0099
51. Crupi F., Magnelli L., Falbo P., **Lanuzza M.**., Nafria M., Rodriguez R. (2007); *"Performance and reliability of ultra-thin oxide nMOSFETs under variable body bias"*. MICROELECTRONIC ENGINEERING, vol. 84, pp. 1947-1950, ISSN: 0167-9317, doi: 10.1016/j.mee.2007.04.015
52. Corsonello P., Perri S., Staino G., **Lanuzza M.**., Cocorullo G. (2006); *"Low bit rate image compression core for onboard space applications"*. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, vol. 16, pp. 114-128, ISSN: 1051-8215, doi: 10.1109/TCSVT.2005.856925
53. Perri S., **Lanuzza M.**., Corsonello P., Cocorullo G. (2005); *"A high-performance fully reconfigurable FPGA-based 2D convolution processor"*. MICROPROCESSORS AND MICROSYSTEMS, Special Issue on FPGAs: Case Studies in Computer Vision and Image Processing, vol. 29, pp. 381-391, ISSN: 0141-9331, doi: 10.1016/j.micpro.2004.10.004
54. Perri S., Corsonello P., Iachino M.A., **Lanuzza M.**., Cocorullo G. (2004); *"Variable precision arithmetic circuits for FPGA-based multimedia processors"*. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, vol. 12, pp. 995-999, ISSN: 1063-8210, doi: 10.1109/TVLSI.2004.833400

INTERNATIONAL CONFERENCES

55. Stanger I., Shavit N., Taco R., Yavits L., **Lanuzza M.**., Fish A. (2020), "Robust Dual Mode Pass Logic (DMPL) for Energy Efficiency and High Performance", In: 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Sevilla, Spain, 10-21 Oct. 2020, pp. 1-4, doi: 10.1109/ISCAS45731.2020.9181127
56. Taco R., Yavits L., Shavit N., Stanger I., **Lanuzza M.**., Fish A. (2020),"Exploiting Single-Well Design for Energy-Efficient Ultra-Wide Voltage Range Dual Mode Logic-Based Digital Circuits in 28nm FD-SOI Technology", In: 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Sevilla, Spain, 10-21 Oct. 2020, pp. 1-4, doi: 10.1109/ISCAS45731.2020.9180449
57. Fassio L., Lin L., De Rose R., **Lanuzza M.**., Crupi F., Alioto M. (2020), " A 0.25-V, 5.3-pW Voltage Reference with 25-µV/°C Temperature Coefficient, 140-µV/V Line Sensitivity and 2,200-µm2 Area in 180nm", In: 2020 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA, USA, 16 – 19 June 2020, doi: 10.1109/VLSICircuits18222.2020.9162872
58. **Lanuzza M.**, De Rose R , Garzon E, Crupi F (2019).Evaluating the Energy Efficiency of STT-MRAMs Based on Perpendicular MTJs with Double Reference Layers. In: 2019 IEEE 13th International Conference on ASIC (ASICON), Chongqing, China, 29 Oct. – 1 Nov. 2019, doi: 10.1109/ASICON47005.2019.8983643, (INVITED)
59. Garzon E, De Rose R , Crupi F, **Lanuzza M.** (2019). Device-to-System Level Simulation Framework for STT-DMTJ Based Cache Memory. In: 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Genova, Italy, 27-29 Nov. 2019, doi:

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BOOK CHAPTERS

101. Palumbo A., Amato F., Calabrese B., Cannataro M., Cocorullo G., Gambardella A., Guzzi P. H., **Lanuzza M.**., Sturniolo M., Veltri P., Vizza P. (2010); "*An embedded system for EEG acquisition and processing for brain computer interface applications*". In: Wearable and Autonomous Biomedical Devices and Systems for Smart Environment. Lecture Notes in Electrical Engineering, Springer Berlin Heidelberg, vol. 75, pp. 137-154, ISBN: 978-3-642-15687-8, Url: http://dx.doi.org/10.1007/978-3-642-15687-8_7

PROFESSIONAL ACTIVITIES

PROFESSIONAL SOCIETY

Institute of Electrical and Electronics Engineers (IEEE) Senior Member (2016-present)
Institute of Electrical and Electronics Engineers (IEEE) Member (2005-2015)

ASSOCIATE EDITOR POSITION

Member of the Editorial Board of the ELSEVIER "Integration, the VLSI Journal" (2013-present)

MISCELLANEOUS INFORMATION

OTHER QUALIFICATIONS

Italian Scientific Qualification for position of Full Professor of Electronics (qualification achieved on December 23, 2019)

DATE JUNE, 23 2021